

## C1812C820KDGACTU

Aliases (C1812C820KDGAC7800) SMD Comm COG HV, Ceramic, 82 pF, 10%, 1,000 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 1812, 2.3 mm



Click here for the 3D model.

General Information	
Series	SMD Comm COG HV
Style	SMD Chip
Description	SMD, MLCC, Ultra-Stable, Low Loss, Class I
Features	Ultra-Stable, Low Loss, Class I
RoHS	Yes
Termination	Tin
Marking	No
AEC-Q200	No
Typical Component Weight	67 mg
Shelf Life	78 Weeks
MSL	1

	Specifications	
	Capacitance	82 pF
	Measurement Condition	1 MHz 1.0Vrms
	Tolerance	10%
	Voltage DC	1000 VDC
	Dielectric Withstanding Voltage	1,200 VDC
	Temperature Range	-55/+125°C
	Temp. Coefficient	COG
	Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1MegaHz 1.0Vrms
	Dissipation Factor	0.1% 1 MHz 1.0Vrms
	Aging Rate	0% Loss/Decade Hour
	Insulation Resistance	100 GOhms

 Dimensions

 Chip Size
 1812

 L
 4.5mm +/-0.3mm

 W
 3.2mm +/-0.3mm

 T
 1mm +/-0.10mm

 S
 2.3mm MIN

 B
 0.6mm +/-0.35mm

# Packaging Specifications Packaging

Packaging T	T&R, 180mm, Plastic Tape
Packaging Quantity 10	000

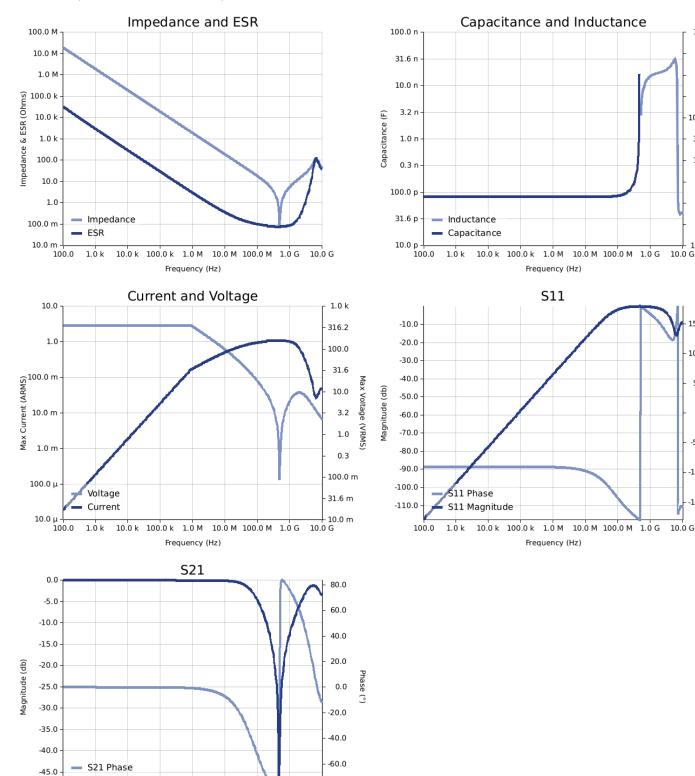
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### Simulations

For the complete simulation environment please visit K-SIM.



-80.0

100.0

-50.0

S21 Magnitude

1.0 k 10.0 k 100.0 k 1.0 M 10.0 M 100.0 M 1.0 G 10.0 G

Frequency (Hz)

10.0 n

3.2 n

1.0 n

0.3 n

100.0 p a

31.6 p 10.0 p 🗄

3.2 p

1.0 p

0.3 p

100.0 f

150.0

100.0

50.0

0.0

-50.0

-100.0

-150.0

10.0 G

Phase

°



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#### These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for hipple klipple current younge vs. requericy plots is the ESR at an bient temperature.
  The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
  The effects shown herein are based on measured data from a multiple part sample of the parts in question.
  Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
  The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages and the part of the parts of the part of the
- generated at any other harmonics.
  Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.