

Aliases (C0402C682K5RAC7867) SMD Comm X7R, Ceramic, 6,800 pF, 10%, 50 VDC, X7R, SMD, MLCC, Temperature Stable, Class II, 0402, 0.3 mm



General Information	
Series	SMD Comm X7R
Style	SMD Chip
Description	SMD, MLCC, Temperature Stable, Class II
Features	Temperature Stable, Class II
RoHS	Yes
Termination	Tin
Marking	No
AEC-Q200	No
Typical Component Weight	1.21 mg
Shelf Life	78 Weeks
MSL	1

6,800 pF

Dimensions	
Chip Size	0402
L	1mm +/-0.05mm
W	0.5mm +/-0.05mm
Т	0.5mm +/-0.05mm
S	0.3mm MIN
В	0.3mm +/-0.1mm

	0.5mm +/-0.05mm	Tolerance	10%	
	0.5mm +/-0.05mm	Voltage DC	50 VDC	
	0.3mm MIN	Dielectric Withstanding Voltage	125 VDC	
	0.3mm +/-0.1mm	Temperature Range	-55/+125°C	
		Temp. Coefficient	X7R	
cifications		Capacitance Change with	15%, 1kHz 1.0Vrms	
	T&R, 180mm, Paper Tape	Reference to +25°C and 0 VDC Applied (TCC)	·	
ntity	10000	Dissipation Factor	2.5%1kHz1.0Vrms	
		Aging Rate	3% Loss/Decade Hour: Referee	

Specifications

Capacitance

L	1mm +/-0.05mm	Measurement Condition	1 kHz 1.0Vrms
W	0.5mm +/-0.05mm	Tolerance	10%
Т	0.5mm +/-0.05mm	Voltage DC	50 VDC
S	0.3mm MIN	Dielectric Withstanding Voltage	125 VDC
В	0.3mm +/-0.1mm	Temperature Range	-55/+125°C
		Temp. Coefficient	X7R
Packaging Specifications		Capacitance Change with	15%, 1kHz 1.0Vrms
Packaging	T&R, 180mm, Paper Tape	Reference to +25°C and 0 VDC Applied (TCC)	
Packaging Quantity	10000		
	10000	Dissipation Factor	2.5% 1 kHz 1.0Vrms
	10000	Dissipation Factor Aging Rate	2.5% 1 kHz 1.0Vrms 3% Loss/Decade Hour: Referee Time is 1000 Hours

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

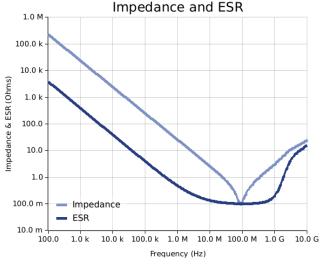
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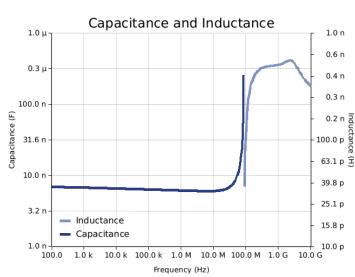


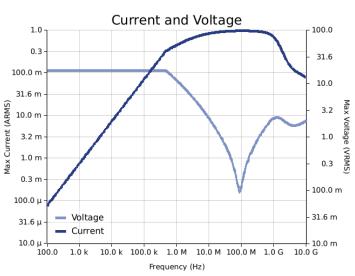
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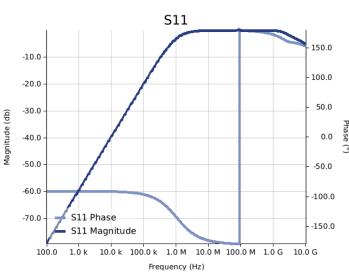
Simulations

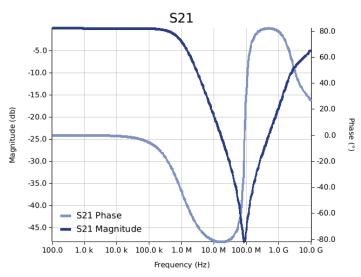
For the complete simulation environment please visit K-SIM.

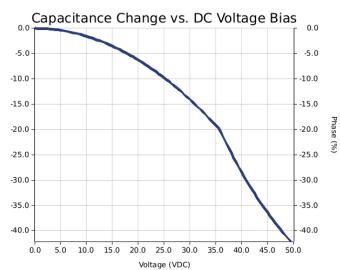










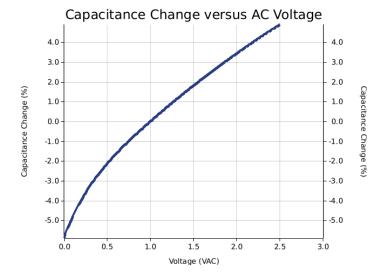


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Phase (%)



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These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for ripple Ripple Currenty votage vs. rrequency plots is unleast at an interact temperature.
 The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
 The effects shown herein are based on measured data from a multiple part sample of the parts in question.
 Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
 The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages
- generated at any other harmonics.

 Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.

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