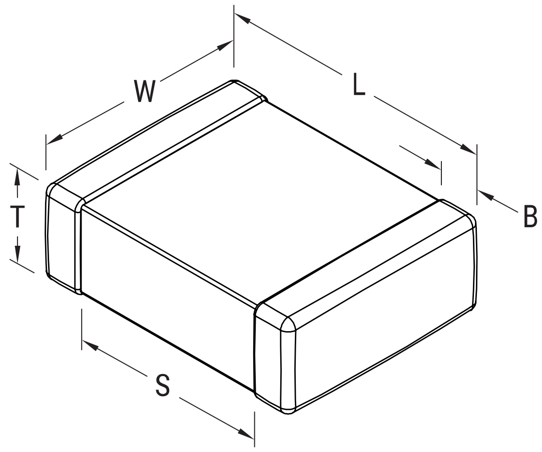
C1210C331GCGAC7210

SMD Comm C0G HV, Ceramic, 330 pF, 2%, 500 VDC, C0G, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 1210, 1.5 mm



Click here for the 3D model.

General Information	
Series	SMD Comm C0G HV
Style	SMD Chip
Description	SMD, MLCC, Ultra-Stable, Low Loss, Class I
Features	Ultra-Stable, Low Loss, Class I
RoHS	Yes
Termination	Tin
Marking	No
AEC-Q200	No
Typical Component Weight	40 mg
Shelf Life	78 Weeks
MSL	1

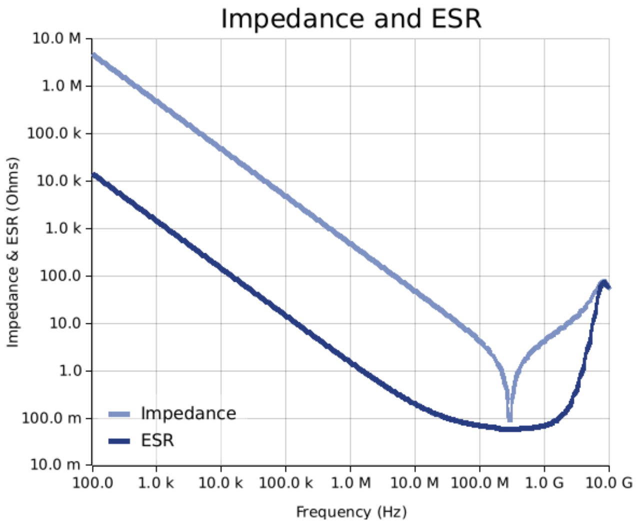
Dimensions	
Chip Size	1210
L	3.2mm +/-0.2mm
W	2.5mm +/-0.2mm
T	1.25mm +/-0.15mm
S	1.5mm MIN
B	0.5mm +/-0.25mm

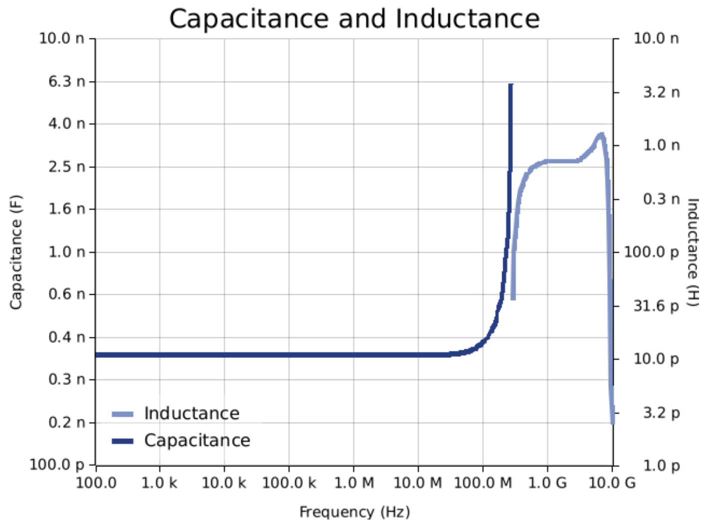
Packaging Specifications	
Packaging	T&R, 330mm, Plastic Tape
Packaging Quantity	10000

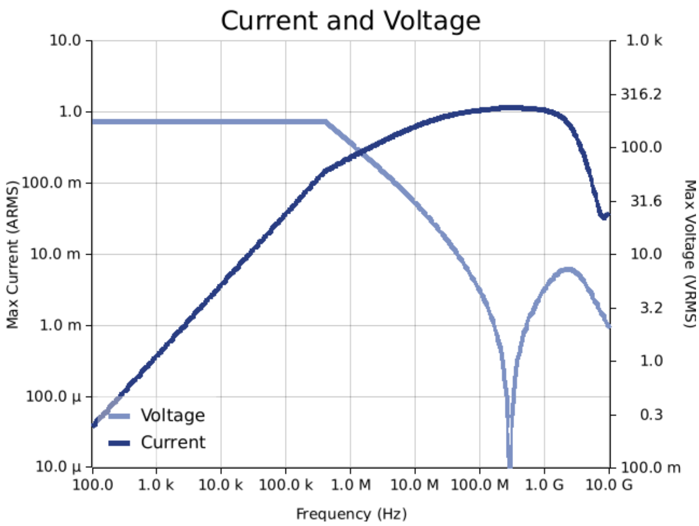
Specifications	
Capacitance	330 pF
Measurement Condition	1 MHz 1.0Vrms
Tolerance	2%
Voltage DC	500 VDC
Dielectric Withstanding Voltage	750 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	C0G
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1MegaHz 1.0Vrms
Dissipation Factor	0.1% 1 MHz 1.0Vrms
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	100 GOhms

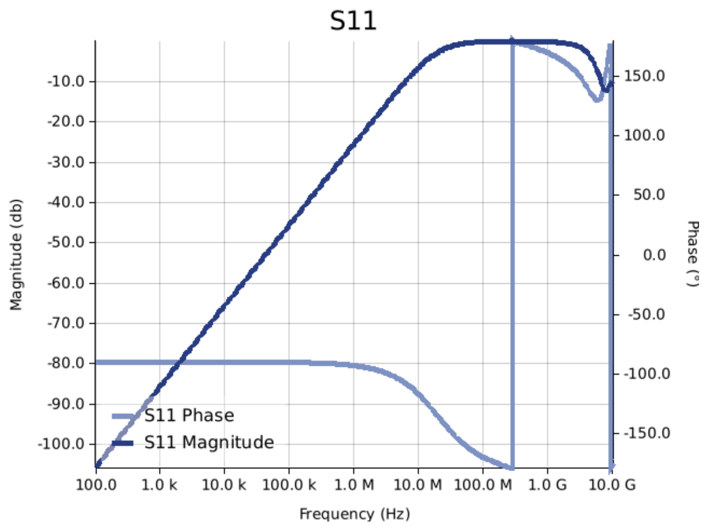
Simulations

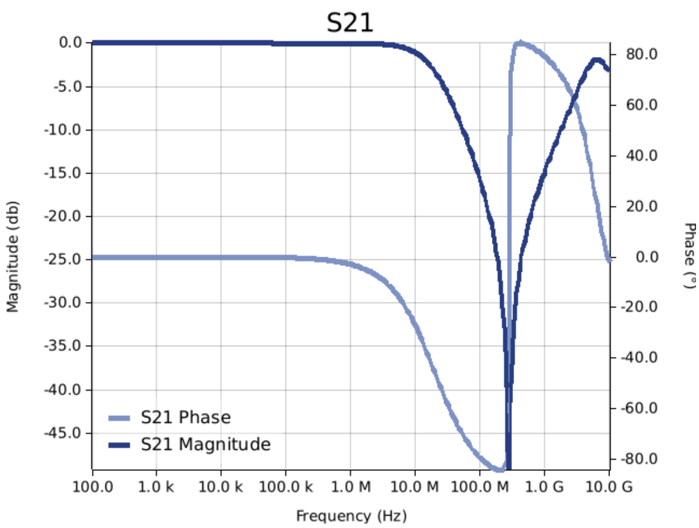
For the complete simulation environment please visit K-SIM.











These are simulations.
This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple “Ripple Current/Voltage vs. Frequency” plots is the ESR at ambient temperature.
- The ESR in the “Temperature Rise vs. Ripple Current” plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the “Temperature Rise vs. Combined Ripple Currents” plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

If you have any questions please contact K-SIM.