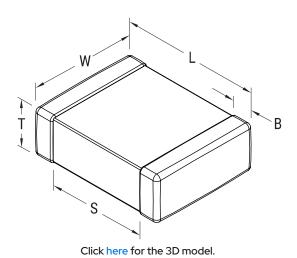


Aliases (C0603C103K5REC7867)

**Specifications** 

Insulation Resistance

ESD SMD Comm X7R, Ceramic, 0.01 uF, 10%, 50 VDC, X7R, SMD, MLCC, Temperature Stable, Electro Static Discharge, Class II, 0603, 0.5 mm



General Information	
Series	ESD SMD Comm X7R
Style	SMD Chip
Description	SMD, MLCC, Temperature Stable, Electro Static Discharge, Class II
Features	Temperature Stable, Class II
RoHS	Yes
Termination	Tin
Marking	No
AEC-Q200	No
Typical Component Weight	4.8 mg
Shelf Life	78 Weeks
MSL	1

Dimensions	
Chip Size	0603
L	1.6mm +/-0.15mm
W	0.8mm +/-0.15mm
Т	0.8mm +/-0.07mm
S	0.5mm MIN
В	0.35mm +/-0.15mm

Capacitance	0.01 uF
Measurement Condition	1 kHz 1.0Vrms
Tolerance	10%
Voltage DC	50 VDC
ESD Level per AEC-Q200	25,000 V ESD Level
Dielectric Withstanding Voltage	125 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	X7R
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	15%, 1kHz 1.0Vrms
Dissipation Factor	2.5% 1 kHz 1.0Vrms
Aging Rate	3% Loss/Decade Hour: Referee Time is 1000 Hours

100 GOhms

Packaging Specifications	
Packaging	T&R, 180mm, Paper Tape
Packaging Quantity	4000

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and
we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the
requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us
with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

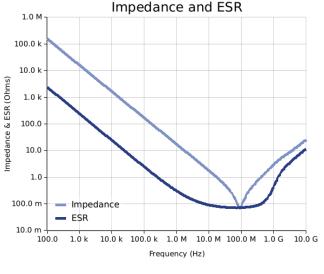
Generated 08/08/2025 © 2006 - 2025 YAGEO

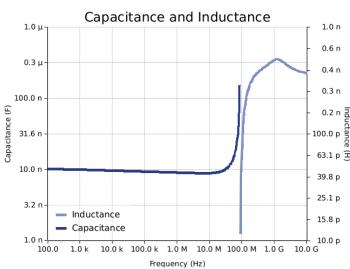


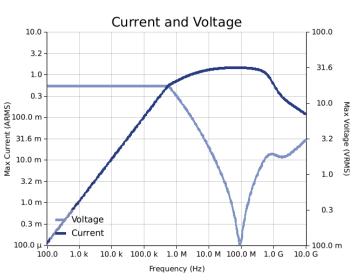
Aliases (C0603C103K5REC7867) ESD SMD Comm X7R, Ceramic, 0.01 uF, 10%, 50 VDC, X7R, SMD, MLCC, Temperature Stable, Electro Static Discharge, Class II, 0603, 0.5 mm

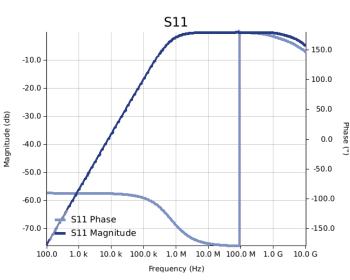
#### **Simulations**

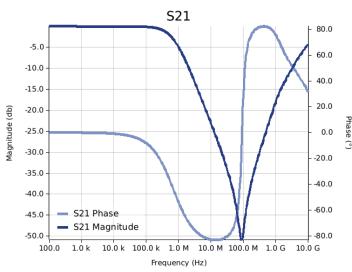
For the complete simulation environment please visit K-SIM.

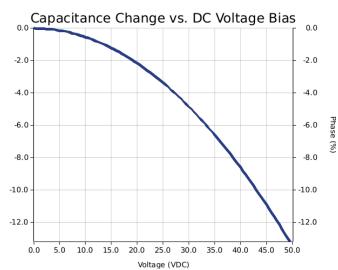










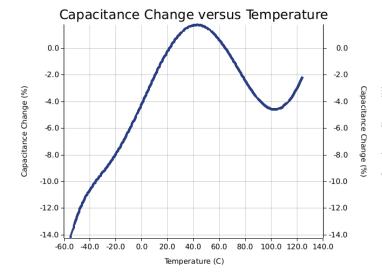


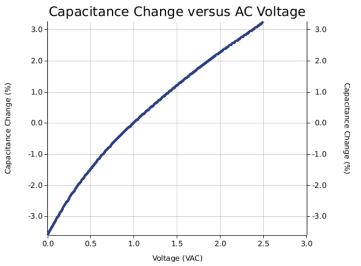
Generated 08/08/2025 © 2006 - 2025 YAGEO

Phase (%)



Aliases (C0603C103K5REC7867) ESD SMD Comm X7R, Ceramic, 0.01 uF, 10%, 50 VDC, X7R, SMD, MLCC, Temperature Stable, Electro Static Discharge, Class II, 0603, 0.5 mm





Generated 08/08/2025 © 2006 - 2025 YAGEO



Aliases (C0603C103K5REC7867)

ESD SMD Comm X7R, Ceramic, 0.01 uF, 10%, 50 VDC, X7R, SMD, MLCC, Temperature Stable, Electro Static Discharge, Class II, 0603, 0.5 mm

#### These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR in the "Temperature Rise vs. Ripple Current" plots is the ESR at ambient temperature. The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated. The effects shown herein are based on measured data from a multiple part sample of the parts in question. Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

  The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages
- generated at any other harmonics.

  Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

All Information given herein is believed to be accurate and reliable, but is presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute – and we specifically disclaim – any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

If you have any questions please contact K-SIM.

Generated 08/08/2025 © 2006 - 2025 YAGEO