

C0805C101KDGACTU

Aliases (C0805C101KDGAC7800) SMD Comm COG HV, Ceramic, 100 pF, 10%, 1,000 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 0805, 0.7 mm



Click here for the 3D model.

General Information	tion	
Series	SMD Comm COG HV	
Style	SMD Chip	
Description	SMD, MLCC, Ultra-Stable, Low Loss, Class I	
Features	Ultra-Stable, Low Loss, Class I	
RoHS	Yes	
Termination	Tin	
Marking	No	
AEC-Q200	No	
Typical Component Weight	14 mg	
Shelf Life	78 Weeks	
MSL	1	

Dimensions		Specificatio
Chip Size	0805	Capacitance
L	2mm +/-0.2mm	Measureme
W	1.25mm +/-0.2mm	Tolerance
т	1.25mm +/-0.15mm	Voltage DC
S	0.7mm MIN	Dielectric Wi
В	0.5mm +/-0.25mm	Temperature
		Temp. Coeff

Packaging Specifications	
Packaging	T&R, 180mm, Plastic Tape
Packaging Quantity	2500

Specifications	
Capacitance	100 pF
Measurement Condition	1 MHz 1.0Vrms
Tolerance	10%
Voltage DC	1000 VDC
Dielectric Withstanding Voltage	1,200 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	COG
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1MegaHz 1.0Vrms
Dissipation Factor	0.1% 1 MHz 1.0Vrms
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	100 GOhms

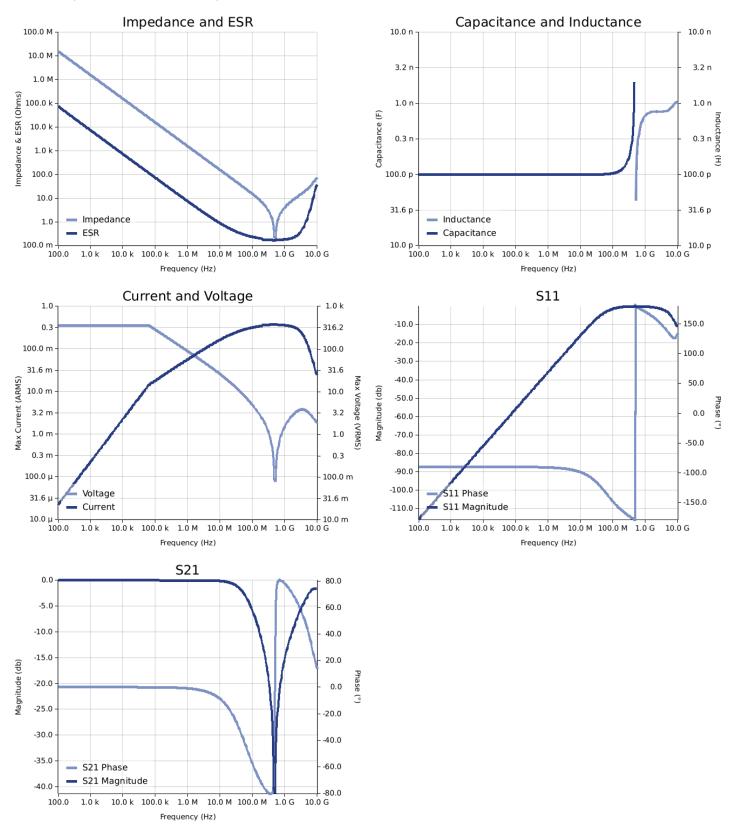
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CO805C101KDGACTU Aliases (C0805C101KDGAC7800) SMD Comm C0G HV, Ceramic, 100 pF, 10%, 1,000 VDC, C0G, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 0805, 0.7 mm

Simulations

For the complete simulation environment please visit K-SIM.





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These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for hipple klipple current younge vs. requericy plots is the ESR at an bient temperature.
 The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
 The effects shown herein are based on measured data from a multiple part sample of the parts in question.
 Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
 The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages are applied to reach previous the burger of the parts.
- generated at any other harmonics. Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.