

C1206C104JMREC

ESD SMD Comm X7R, Ceramic, 0.1 uF, 5%, 63 VDC, X7R, SMD, MLCC, Temperature Stable, Electro Static Discharge, Class II, 1206, 1.5 mm



Click [here](#) for the 3D model.

General Information

| | |
|--------------------------|---|
| Series | ESD SMD Comm X7R |
| Style | SMD Chip |
| Description | SMD, MLCC, Temperature Stable, Electro Static Discharge, Class II |
| Features | Temperature Stable, Class II |
| RoHS | Yes |
| Termination | Tin |
| Marking | No |
| AEC-Q200 | No |
| Typical Component Weight | 31 mg |
| Shelf Life | 78 Weeks |
| MSL | 1 |

Specifications

| | |
|--|---|
| Capacitance | 0.1 uF |
| Measurement Condition | 1 kHz 1.0Vrms |
| Tolerance | 5% |
| Voltage DC | 63 VDC |
| ESD Level per AEC-Q200 | 25,000 V ESD Level |
| Dielectric Withstanding Voltage | 157.5 VDC |
| Temperature Range | -55/+125°C |
| Temp. Coefficient | X7R |
| Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC) | 15%, 1kHz 1.0Vrms |
| Dissipation Factor | 2.5% 1 kHz 1.0Vrms |
| Aging Rate | 3% Loss/Decade Hour: Referee Time is 1000 Hours |
| Insulation Resistance | 10 GOhms |

Dimensions

| | |
|-----------|------------------|
| Chip Size | 1206 |
| L | 3.2mm +/-0.2mm |
| W | 1.6mm +/-0.2mm |
| T | 1.25mm +/-0.15mm |
| S | 1.5mm MIN |
| B | 0.5mm +/-0.25mm |

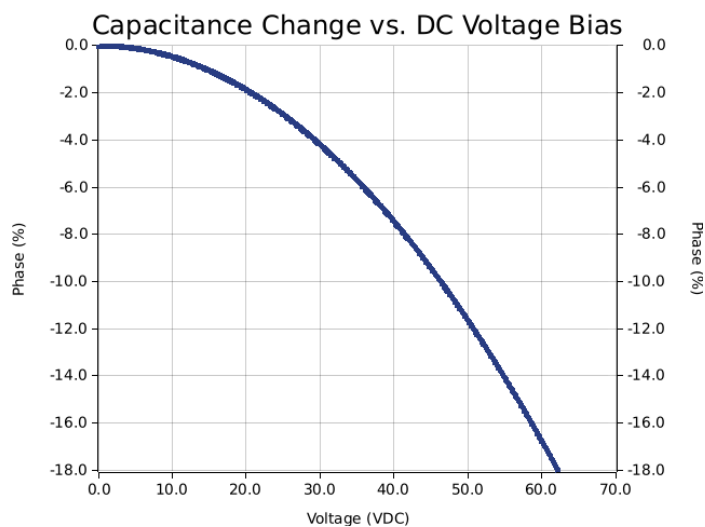
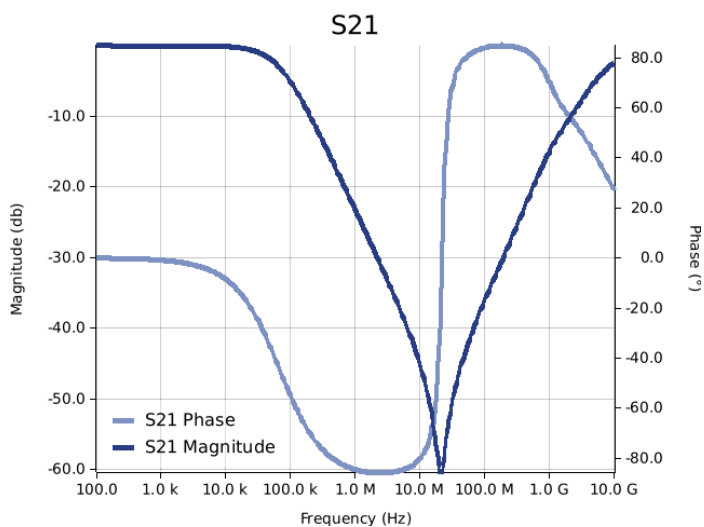
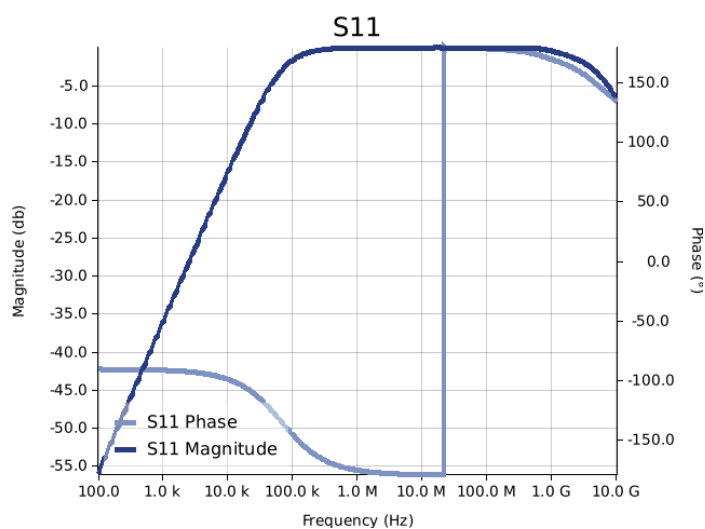
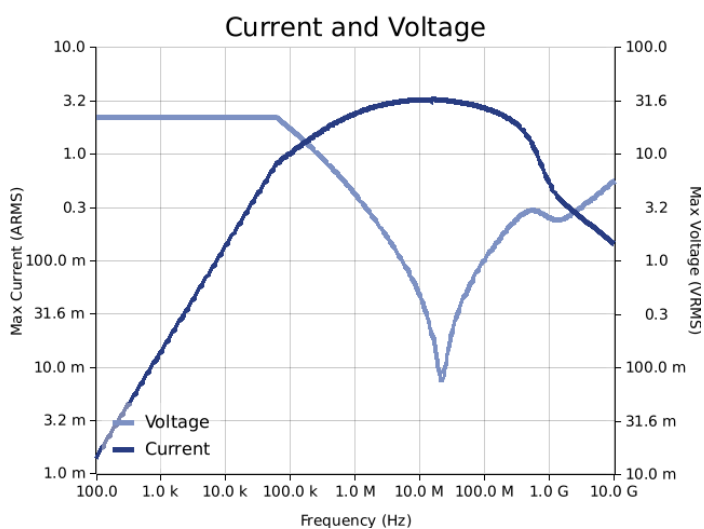
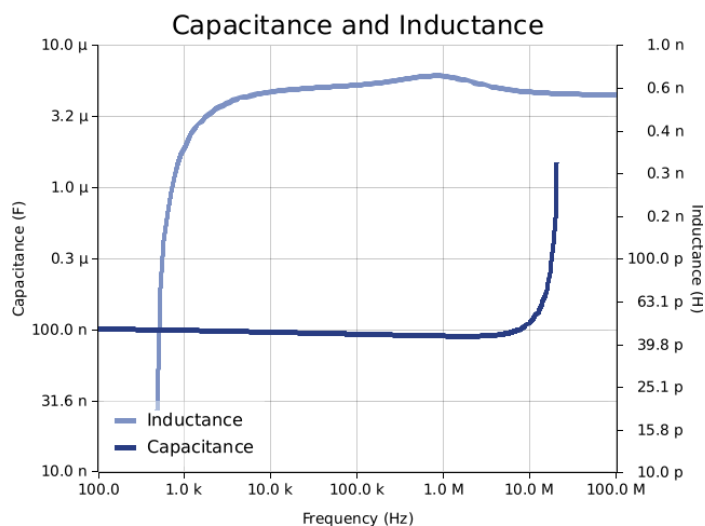
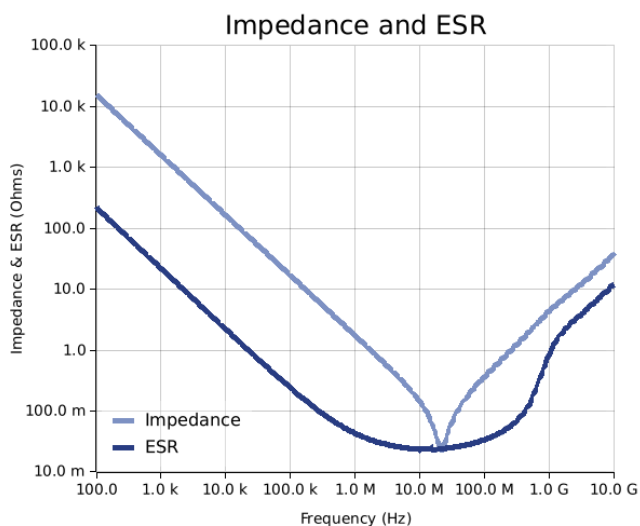
Packaging Specifications

| | |
|--------------------|-----------|
| Packaging | Bulk, Bag |
| Packaging Quantity | 1 |

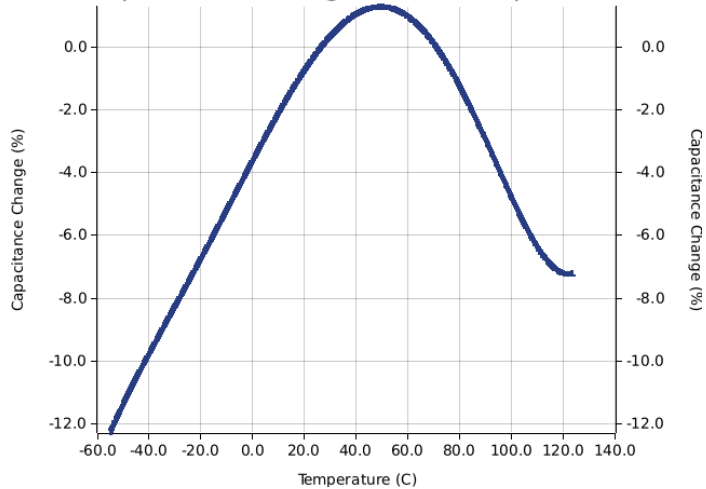
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Simulations

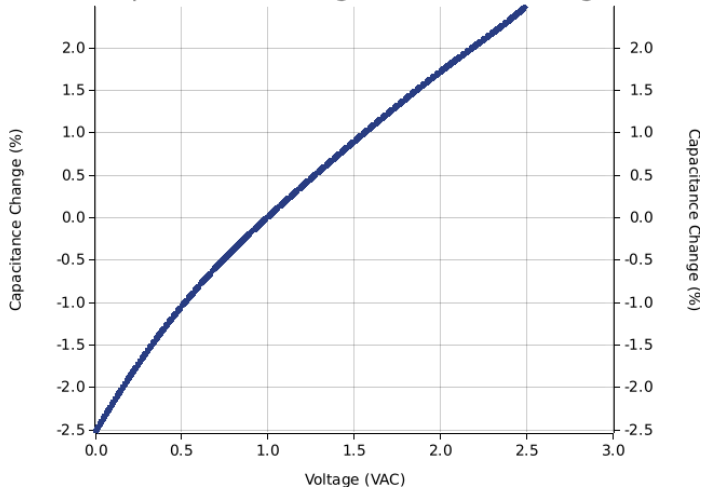
For the complete simulation environment please visit [Y-SIM](#).



Capacitance Change versus Temperature



Capacitance Change versus AC Voltage



These are simulations.
This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (R_{th}) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance).
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.