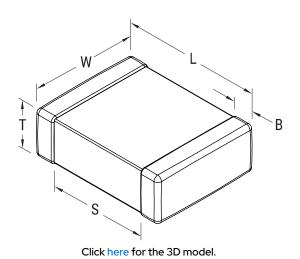


# C1812C104K5GACTU

Aliases (C1812C104K5GAC7800) SMD Comm COG, Ceramic, 0.1 uF, 10%, 50 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 1812, 2.3 mm



General Information		
Series	SMD Comm COG	
Style	SMD Chip	
Description	SMD, MLCC, Ultra-Stable, Low Loss, Class I	
Features	Ultra-Stable, Low Loss, Class I	
RoHS	Yes	
Termination	Tin	
Marking	No	
AEC-Q200	No	
Typical Component Weight	67 mg	
Shelf Life	78 Weeks	
MSL	1	

0.1 uF

Dimensions	
Chip Size	1812
L	4.5mm +/-0.3mm
W	3.2mm +/-0.3mm
Т	1mm +/-0.10mm
S	2.3mm MIN
В	0.6mm +/-0.35mm

	4.5mm +/-0.3mm	Measurement Condition	1 kHz 1.0Vrms
	3.2mm +/-0.3mm	Tolerance	10%
	1mm +/-0.10mm	Voltage DC	50 VDC
	2.3mm MIN	Dielectric Withstanding Voltage	125 VDC
	0.6mm +/-0.35mm	Temperature Range	-55/+125°C
		Temp. Coefficient	COG
ifications	T&R, 180mm, Plastic Tape	Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1kHz 1.0Vrms
tity	1000	Dissipation Factor	0.1% 1 kHz 1.0Vrms
		Aging Rate	0% Loss/Decade Hour

**Specifications** 

Capacitance

'	111111 +/ -0.10111111	voitage DC	30 VDC
S	2.3mm MIN	Dielectric Withstanding Voltage	125 VDC
В	0.6mm +/-0.35mm	Temperature Range	-55/+125°C
		Temp. Coefficient	COG
Packaging Specifications		Capacitance Change with	30 ppm/C, 1kHz 1.0Vrms
Packaging	T&R, 180mm, Plastic Tape	Reference to +25°C and 0 VDC Applied (TCC)	, ,
Packaging Quantity 1000	1000	Dissipation Factor	0.1% 1 kHz 1.0Vrms
		Aging Rate	0% Loss/Decade Hour
		Insulation Resistance	10 GOhms

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

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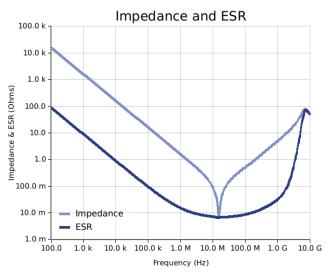


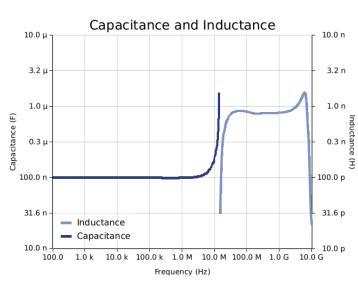
## C1812C104K5GACTU

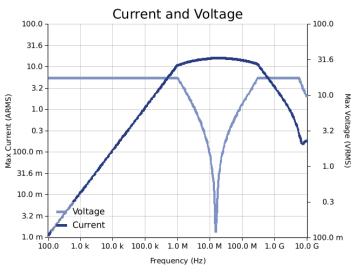
Aliases (C1812C104K5GAC7800) SMD Comm COG, Ceramic, 0.1 uF, 10%, 50 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 1812, 2.3 mm

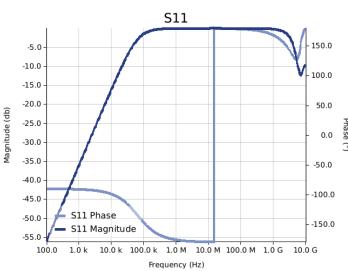
### **Simulations**

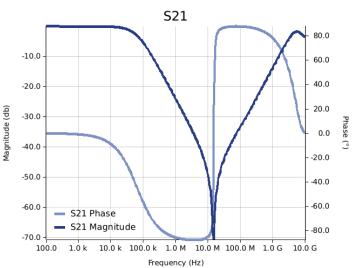
For the complete simulation environment please visit K-SIM.











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### C1812C104K5GACTU

Aliases (C1812C104K5GAC7800) SMD Comm COG, Ceramic, 0.1 uF, 10%, 50 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 1812, 2.3 mm

#### These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for ripple Ripple Currenty votage vs. rrequency plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
  The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
  The effects shown herein are based on measured data from a multiple part sample of the parts in question.
  Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
  The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages
- generated at any other harmonics.

   Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

All Information given herein is believed to be accurate and reliable, but is presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute – and we specifically disclaim – any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

If you have any questions please contact K-SIM.

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