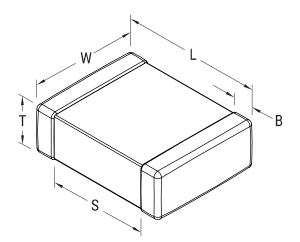


CKC18X103KWGAC7210

KC-LINK Comm COG, Ceramic, 0.01 uF, 10%, 650 VDC, COG, SMD, MLCC, FT-CAP, Ultra-Stable, 1812



Click here for the 3D model.

General Information		
Series	KC-LINK Comm COG	
Style	SMD Chip	
Description	SMD, MLCC, FT-CAP, Ultra- Stable	
Features	FT-CAP, Ultra-Stable	
RoHS	Yes	
Termination	Flexible Termination	
Marking	No	
AEC-Q200	No	
Typical Component Weight	87 mg	
Shelf Life	78 Weeks	
MSL	1	

	Specifications	
1812	Capacitance	0.01 uF
4.5mm +/-0.4mm	Measurement Condition	1 kHz 1.0Vrms
3.2mm +/-0.3mm	Tolerance	10%
2mm +/-0.20mm	Voltage DC	650 VDC
0.7mm +/-0.35mm	Dielectric Withstanding Voltage	845 VDC
	Temperature Range	-55/+150°C
	Temp. Coefficient	COG
T&R, 330mm, Plastic Tape	Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1kHz 1.0Vrms
2000		
	Dissipation Factor	0.1% 1 kHz 1.0Vrms
	Aging Pata	0% Loss /Docado Hour

Aging Rate 0% Loss/Decade Hour 100 GOhms Insulation Resistance

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute – and we specifically disclaim – any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

Dimensions

Packaging Specifications

Packaging Quantity

Chip Size

Packaging

L W

Т

В

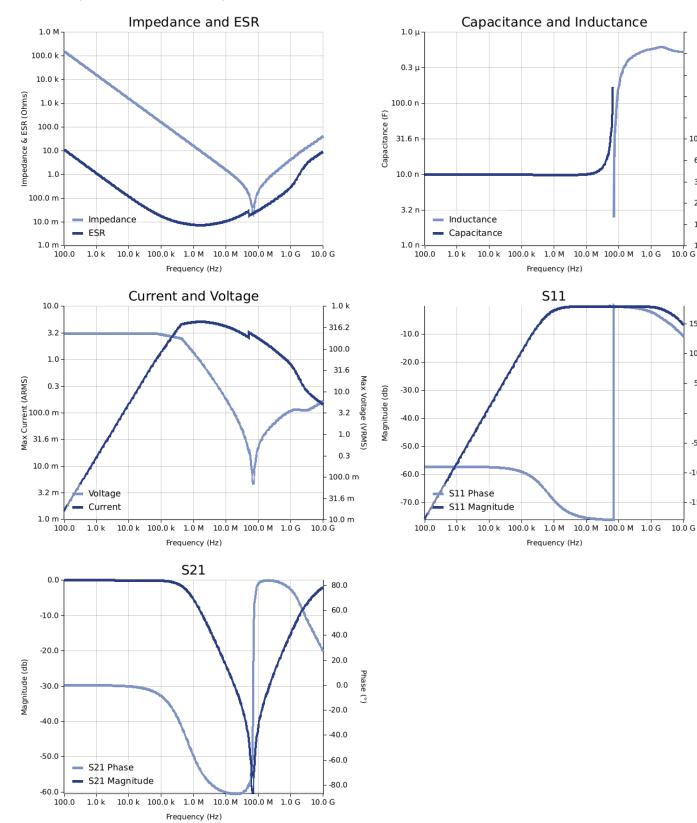


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Simulations

For the complete simulation environment please visit Y-SIM.



1.0 n

0.6 n

0.4 n

0.3 n

100.0 p

0.2 n a

63.1 p 🗄

39.8 p

25.1 p

15.8 p

10.0 p

150.0

100.0

50.0

0.0

-50.0

-100.0

-150.0

Phase (°)



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These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for https:// temperature Rise vs. Ripple Current/ voltage vs. Frequency plots is the ESR at ambient temperature.
 The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
 The effects shown herein are based on measured data from a multiple part sample of the parts in question.
 Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
 The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages
- generated at any other harmonics.
 Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.