

CKC18X472JCGACTU

Aliases (CKC18X472JCGAC7800) KC-LINK Comm COG, Ceramic, 4,700 pF, 5%, 500 VDC, COG, SMD, MLCC, FT-CAP, Ultra-Stable, 1812



General Information	
Series	KC-LINK Comm COG
Style	SMD Chip
Description	SMD, MLCC, FT-CAP, Ultra- Stable
Features	FT-CAP, Ultra-Stable
RoHS	Yes
Termination	Flexible Termination
Marking	No
AEC-Q200	No
Typical Component Weight	67 mg
Shelf Life	78 Weeks
MSL	1

Specifications 4,700 pF Capacitance Measurement Condition 1 kHz 1.0Vrms Tolerance 5% Voltage DC 500 VDC **Dielectric Withstanding Voltage** 750 VDC **Temperature Range** -55/+150°C Temp. Coefficient COG 30 ppm/C, 1kHz 1.0Vrms Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC) 0.1% 1 kHz 1.0Vrms **Dissipation Factor** 0% Loss/Decade Hour Aging Rate Insulation Resistance 100 GOhms

 Dimensions

 Chip Size
 1812

 L
 4.5mm +/-0.4mm

 W
 3.2mm +/-0.3mm

 T
 1.25mm +/-0.15mm

 B
 0.7mm +/-0.35mm

Click here for the 3D model.

Packaging Specifications	
Packaging	T&R, 180mm, Plastic Tape
Packaging Quantity	1000

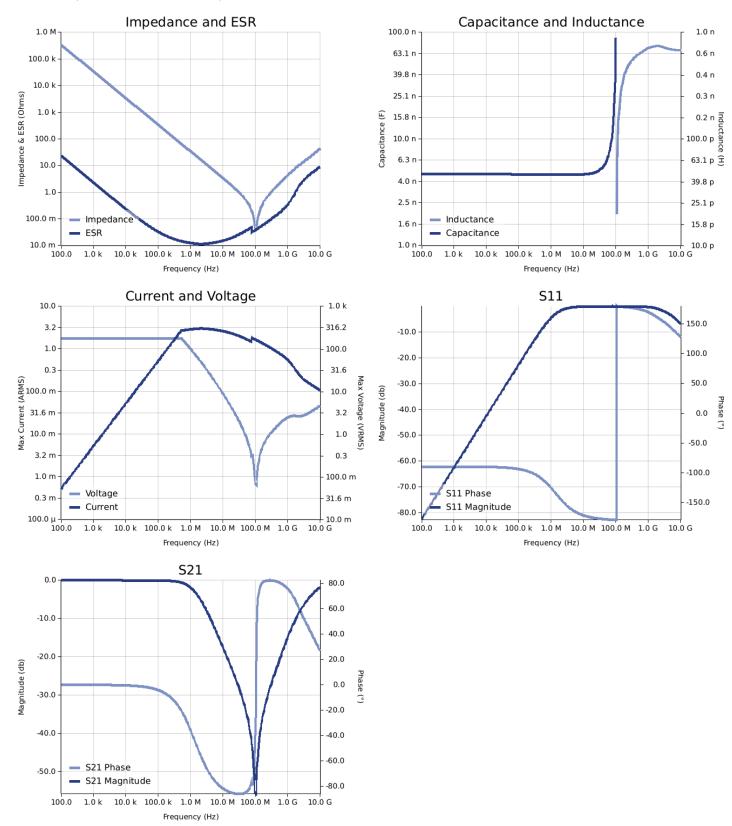
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Simulations

For the complete simulation environment please visit K-SIM.





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These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for hipple klipple current younge vs. requericy plots is the ESR at an bient temperature.
 The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
 The effects shown herein are based on measured data from a multiple part sample of the parts in question.
 Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
 The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages and the part of the parts of the part of the
- generated at any other harmonics. Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.