

CKC21C562JEGACTU

Aliases (CKC21C562JEGAC7800) KC-LINK Comm COG, Ceramic, 5,600 pF, 5%, 1,200 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 2220, 3.5 mm



General Information	
Series	KC-LINK Comm COG
Style	SMD Chip
Description	SMD, MLCC, Ultra-Stable, Low Loss, Class I
Features	Ultra-Stable, Low Loss, Class I
RoHS	Yes
Termination	Tin
Marking	No
AEC-Q200	No
Typical Component Weight	260 mg
Shelf Life	78 Weeks
MSL	1

Dimensions	
Chip Size	2220
L	5.7mm +/-0.4mm
W	5mm +/-0.4mm
Т	2mm +/-0.20mm
S	3.5mm MIN
В	0.6mm +/-0.35mm

W	5mm +/-0.4mm	Tolerance	5%
Т	2mm +/-0.20mm	Voltage DC	1200 VDC
S	3.5mm MIN	Dielectric Withstanding Voltage	1,440 VDC
В	0.6mm +/-0.35mm	Temperature Range	-55/+150°C
		Temp. Coefficient	COG
Packaging Specifications		Capacitance Change with	30 ppm/C, 1kHz 1.0Vrms
Packaging	T&R, 180mm, Plastic Tape	Reference to +25°C and 0 VDC Applied (TCC)	, .
Packaging Quantity	500	Dissipation Factor	0.1% 1 kHz 1.0Vrms
		Dissipation actor	0.170 TRI 12 1.0 VIII.3
		Aging Rate	0% Loss/Decade Hour

Specifications	
Capacitance	5,600 pF
Measurement Condition	1 kHz 1.0Vrms
Tolerance	5%
Voltage DC	1200 VDC
Dielectric Withstanding Voltage	1,440 VDC
Temperature Range	-55/+150°C
Temp. Coefficient	COG
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1kHz 1.0Vrms
Dissipation Factor	0.1% 1 kHz 1.0Vrms
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	100 GOhms

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

Generated 06/19/2025 © 2006 - 2025 YAGEO

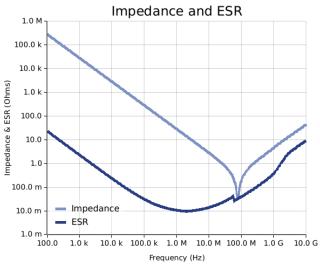


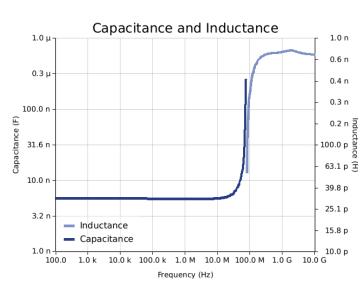
CKC21C562JEGACTU

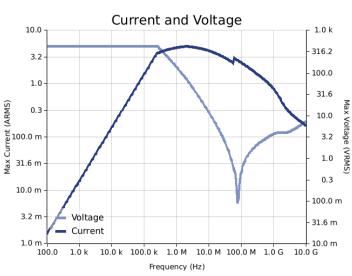
Aliases (CKC21C562JEGAC7800) KC-LINK Comm COG, Ceramic, 5,600 pF, 5%, 1,200 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 2220, 3.5 mm

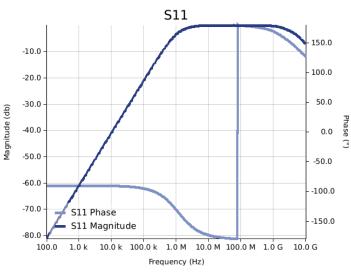
Simulations

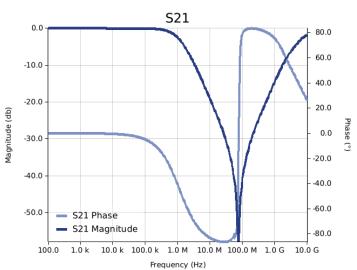
For the complete simulation environment please visit K-SIM.











Generated 06/19/2025 © 2006 - 2025 YAGEO



CKC21C562JEGACTU

Aliases (CKC21C562JEGAC7800) KC-LINK Comm COG, Ceramic, 5,600 pF, 5%, 1,200 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 2220, 3.5 mm

These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for ripple Ripple Currenty votage vs. rrequency plots is unleast at an interact temperature.
 The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
 The effects shown herein are based on measured data from a multiple part sample of the parts in question.
 Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
 The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages
- generated at any other harmonics.

 Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

All Information given herein is believed to be accurate and reliable, but is presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute – and we specifically disclaim – any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

If you have any questions please contact K-SIM.

Generated 06/19/2025 © 2006 - 2025 YAGEO