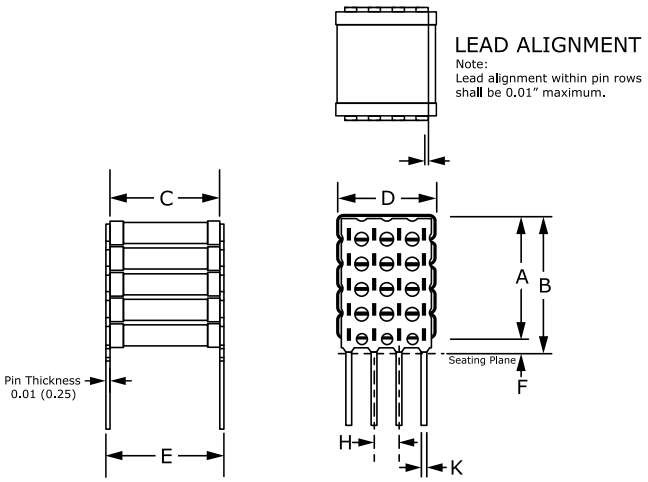
L1GN40D274KA05

KPS-MCC Indust C0G HT200C, Ceramic, 0.27 uF, 10%, 1,000 VDC, C0G



Click here for the 3D model.

General Information	
Series	KPS-MCC Indust C0G HT200C
Style	Leaded Stacked Chip
Description	Low ESR, Stacked Ceramic Chips
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance
RoHS	With Exemptions
REACH	SVHC (Pb – CAS 7439-92-1)
SCIP Number	297427bb-2a48-4853-b594-641304a2cc24
Termination	Silver
Lead	Straight Leads
AEC-Q200	No
Notes	Number of chips in this stack: 5.

Dimensions	
D	10.16mm +/-0.635mm
L	6.35mm MIN
H	2.54mm NOM
F	1.397mm +/-0.25mm
A	13.46mm MAX
B	15.238mm MAX
C	10.16mm +/-0.635mm
E	11.18mm MAX
K	0.5mm NOM

Specifications	
Capacitance	0.27 uF
Tolerance	10%
Voltage DC	1000 VDC
Dielectric Withstanding Voltage	1,200 VDC
Temperature Range	-55/+200°C
Temp. Coefficient	C0G
Dissipation Factor	0.1% 1 kHz 25C
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	3.7 GOhms

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	16

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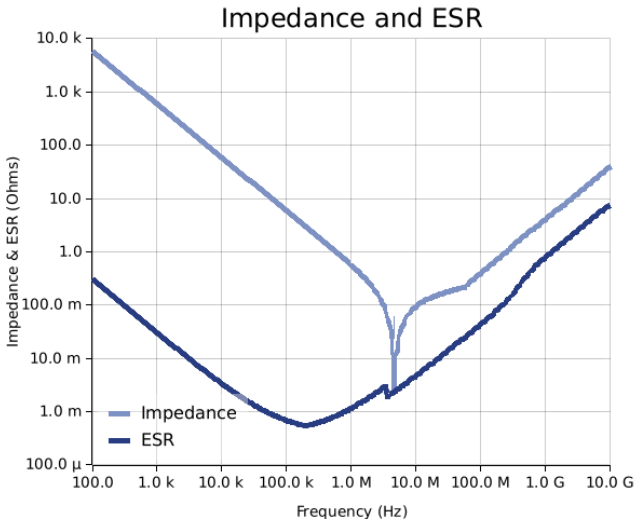
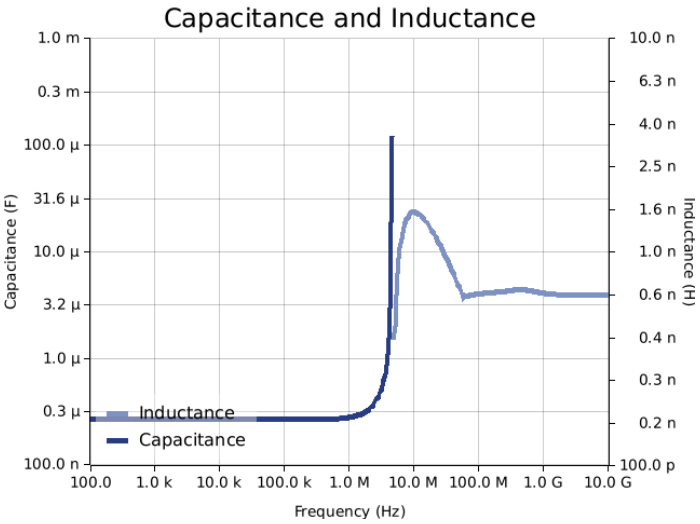
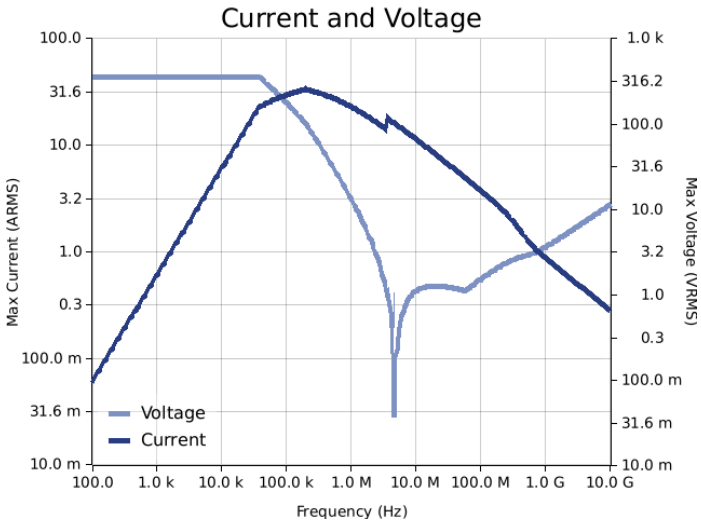
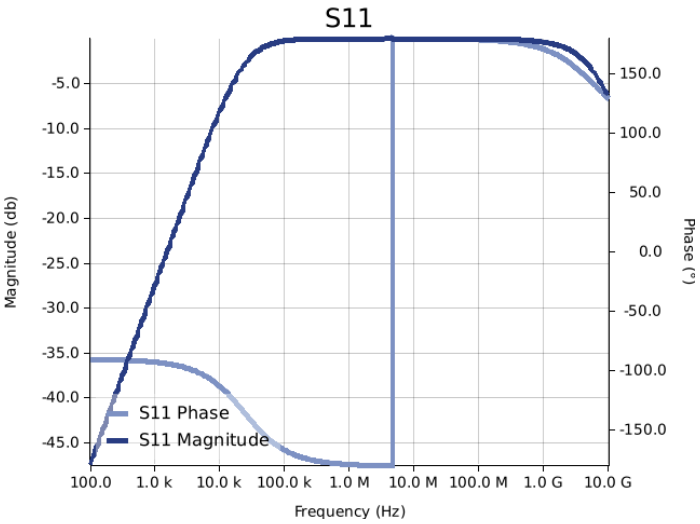
Simulations

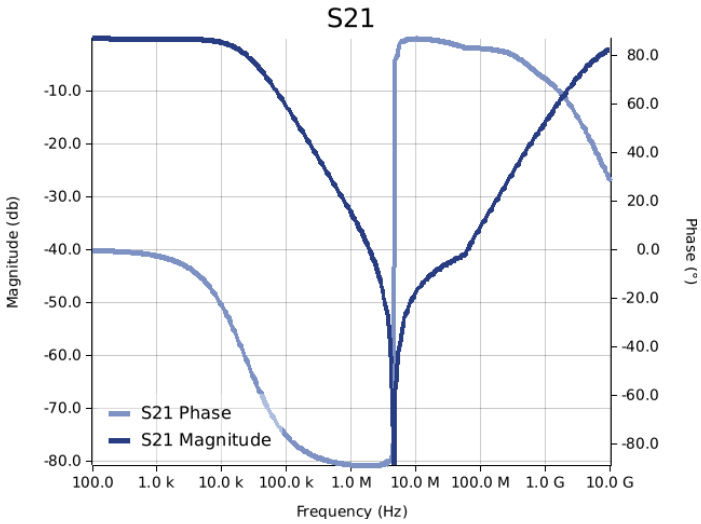
For the complete simulation environment please visit K-SIM.











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These are simulations.
This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.